What is claimed is:

1. A European digital audio broadcast receiver having diverse fast Fourier transform (FFT) modes based on sizes of transmitted data, comprising:

an address generator for generating a predetermined number of write addresses and read addresses;

a fast Fourier transform (FFT) processor for repeating data of FFT modes to generate a predetermined number of data and implementing a fast Fourier transform (FFT) by using the predetermined number of data; and

a controller for controlling the address generator to the write addresses and the read addresses according to operations of the FFT processor.

2. The receiver as claimed in claim 1, wherein the predetermined number of data is 4096, and the FFT processor uses the 4096 data to implement the fast Fourier transform.

3. The receiver as claimed in claim 1, wherein the FFT processor includes:

a memory controller for repeating the data of FFT modes to generate 4096 data;

a memory having a size capable of storing 2048 data; and

an algorithm unit for using the 4096 data and implementing Radix-4 based operations, and, in the case that the read addresses are generated, the

memory controller digit-reverses the addresses of the memory in correspondence to the read addresses.

4. The receiver as claimed in claim 3, wherein the memory controller has a virtual memory storing other than the 2048 data stored in the memory in order for the algorithm unit to implement the Radix-4 based operations.

5. The receiver as claimed in claim 4, wherein the algorithm unit implements the Radix-4 based operations, and, accordingly, "0" data blocks are stored in the virtual memory in correspondence to the FFT modes.

6. The receiver as claimed in claim 3, wherein the memory controller digit-reverses the data operated on based on the Radix-4 algorithm and stored in the memory corresponding to the FFT modes.

7. The receiver as claimed in claim 3, wherein, in the case that a bit array of the read addresses from a highest bit to a lowest bit has $\{a_{11}, a_{10}, a_9, a_8, a_7, a_6, a_5, a_4, a_3, a_2, a_1, a_0\}$ in 2048 FFT mode, the memory controller digit-reverses the bit array of the memory addresses from the highest bit to the lowest bit into $\{a_1, a_3, a_2, a_5, a_4, a_7, a_6, a_9, a_8, a_{11}, a_{10}\}$.

8. The receiver as claimed in claim 3, wherein, in the case that a bit array of the read addresses from a highest bit to a lowest bit has $\{a_{11}, a_{10}, a_9, a_8, a_7, a_6, a_5, a_4, a_3, a_2, a_1, a_0\}$ in 1024 FFT mode, the memory controller

digit-reverses the bit array of the memory addresses from the highest bit to the lowest bit into $\{0, a_3, a_2, a_5, a_4, a_7, a_6, a_9, a_8, a_{11}, a_{10}\}$.

9. The receiver as claimed in claim 3, wherein, in the case that a bit array of the read addresses from a highest bit to a lowest bit has $\{a_{11}, a_{10}, a_9, a_8, a_7, a_6, a_5, a_4, a_3, a_2, a_1, a_0\}$ in 256 FFT mode, the memory controller digit-reverses the bit array of the memory addresses from the highest bit to the lowest bit into $\{0, 0, 0, a_5, a_4, a_7, a_6, a_9, a_8, a_{11}, a_{10}\}$.

10. The receiver as claimed in claim 3, wherein, in the case that a bit array of the read addresses from a highest bit to a lowest bit has $\{a_{11}, a_{10}, a_9, a_8, a_7, a_6, a_5, a_4, a_3, a_2, a_1, a_0\}$ in 512 FFT mode, the memory controller digit-reverses the bit array of the memory addresses from the highest bit to the lowest bit into $\{0, a_3, 0, a_5, a_4, a_7, a_6, a_9, a_8, a_{11}, a_{10}\}$.

11. An operation method for a European digital audio broadcast receiver having diverse FFT modes based on sizes of transmitted data, comprising steps of:

generating a predetermined number of write addresses;

repeating data of FFT modes to generate a predetermined number of data in correspondence to the write addresses, and implementing a fast Fourier transform (FFT) by using the predetermined number of data; and

generating read addresses if the operation of the FFT step is completed.

12. The operation method as claimed in claim 11, wherein the predetermined number of data is 4096, and the FFT step uses the 4096 data to implement the fast Fourier transform.

13. The operation method as claimed in claim 11, wherein the FFT step includes steps of:

repeating the data of FFT modes to generate 4096 data;

using the 4096 data to implement Radix-4 based operations, and storing the implemented data in a memory in correspondence to addresses of the memory; and

digit-reversing, in the case that the read addresses are generated, the read addresses to the addresses of the memory corresponding to the read addresses.

14. The operation method as claimed in claim 13, further comprising a step of storing the 4096 data repeated in the operation step in the memory and a virtual memory for the Radix-4 based operations.

15. The operation method as claimed in claim 14, wherein the operation step implements the Radix-4 based operations, and, accordingly, "0" data blocks are stored in the virtual memory in correspondence to the FFT modes.

16. The operation method as claimed in claim 13, wherein the digit-reversing step digit-reverses the data operated on based on the Radix-4 algorithm and stored in the memory corresponding to the FFT modes.

17. The operation method as claimed in claim 13, wherein, in the case that a bit array of the read addresses from a highest bit to a lowest bit has $\{a_{11}, a_{10}, a_9, a_8, a_7, a_6, a_5, a_4, a_3, a_2, a_1, a_0\}$ in 2048 FFT mode, the digit-reversing step digit-reverses the bit array of the memory addresses from the highest bit to the lowest bit into $\{a_1, a_3, a_2, a_5, a_4, a_7, a_6, a_9, a_8, a_{11}, a_{10}\}$.

18. The operation method as claimed in claim 13, wherein, in the case that a bit array of the read addresses from a highest bit to a lowest bit has $\{a_{11}, a_{10}, a_9, a_8, a_7, a_6, a_5, a_4, a_3, a_2, a_1, a_0\}$ in 1024 FFT mode, the digit-reversing step digit-reverses the bit array of the memory addresses from the highest bit to the lowest bit into $\{0, a_3, a_2, a_5, a_4, a_7, a_6, a_9, a_8, a_{11}, a_{10}\}$.

19. The operation method as claimed in claim 13, wherein, in the case that a bit array of the read addresses from a highest bit to a lowest bit has $\{a_{11}, a_{10}, a_9, a_8, a_7, a_6, a_5, a_4, a_3, a_2, a_1, a_0\}$ in 256 FFT mode, the digit-reversing step digit-reverses the bit array of the memory addresses from the highest bit to the lowest bit into $\{0, 0, 0, a_5, a_4, a_7, a_6, a_9, a_8, a_{11}, a_{10}\}$.

20. The operation method as claimed in claim 13, wherein, in the case that a bit array of the read addresses from a highest bit to a lowest bit has $\{a_{11}, a_{10}, a_9, a_8, a_7, a_6, a_5, a_4, a_3, a_2, a_1, a_0\}$ in 512 FFT mode, the digit-reversing

step digit-reverses the bit array of the memory addresses from the highest bit to the lowest bit into $\{0, a_3, 0, a_5, a_4, a_7, a_6, a_9, a_8, a_{11}, a_{10}\}$.